μA702B
HIGH GAIN, WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

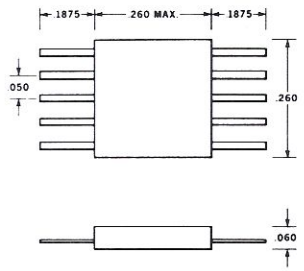
GENERAL DESCRIPTION — The μA702B is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For improved specifications, see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

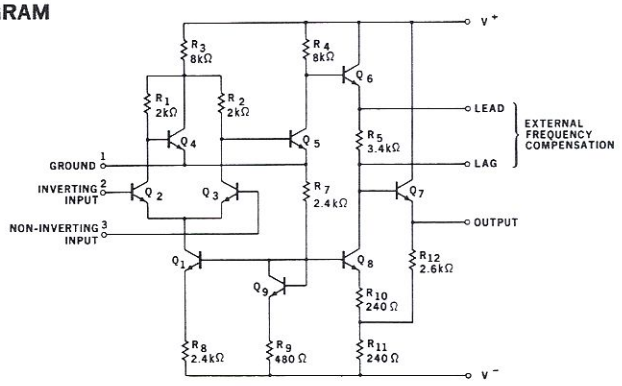
Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55° C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

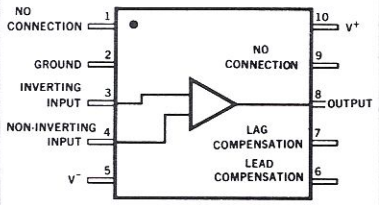


ORDER PART NO.
U3H7702313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

NOTE 1: Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

*Planar is a patented Fairchild process.

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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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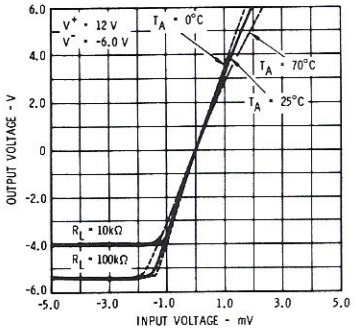
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

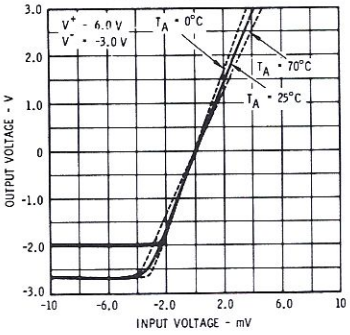
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2000	3400	6000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_1 = 0.01\ \mu F$, $R_1 = 20\Omega$, $R_L \leq 100\ k\Omega$, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100\ k\Omega$, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = +70°C$ to $T_A = 0°C$		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		4.0	10		3.0	8.0	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0°C$		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = 6$ V to $V^+ = 6$ V, $V^- = 3$ V, $R_S \leq 2\ k\Omega$		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1500		7000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				400		1750	
The following specifications apply for −55°C ≤ T_A ≤ +125°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			7.5			8.0	mV
Input Offset Current	$T_A = +125°C$		0.2	2.0		0.14	2.0	μA
	$T_A = -55°C$		1.2	4.0		0.8	4.0	μA
Input Bias Current	$T_A = -55°C$		5.5	20		3.4	15	μA
Input Resistance		3.0			4.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	60	80		60	80		dB
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1200						
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				300			
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{out} = 0$		90	135		19	35	mW

TYPICAL PERFORMANCE CURVES

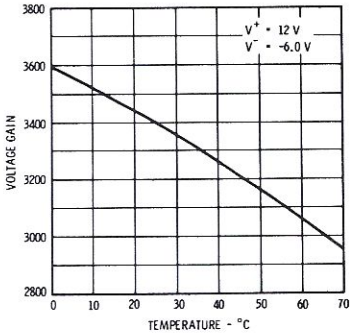
VOLTAGE TRANSFER CHARACTERISTIC



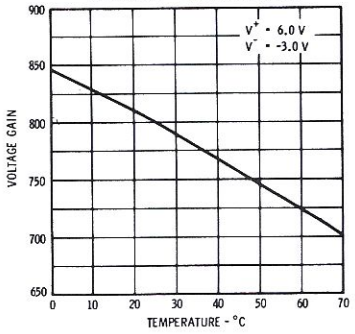
VOLTAGE TRANSFER CHARACTERISTIC



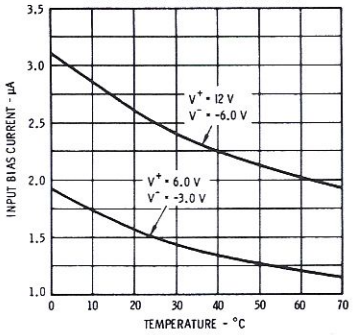
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



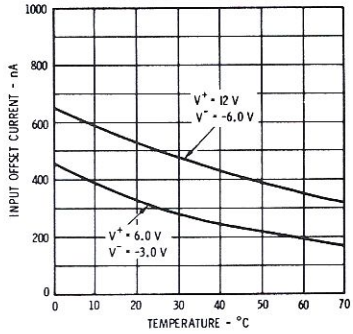
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



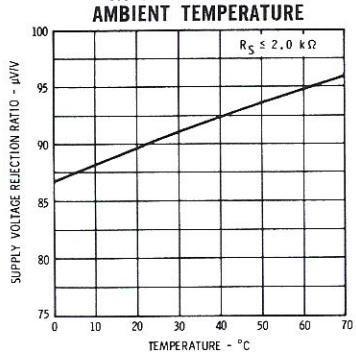
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



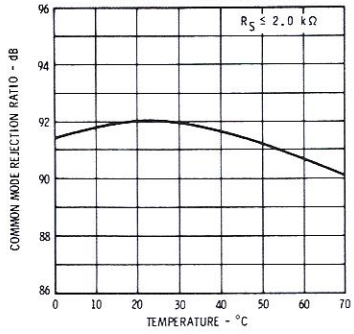
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



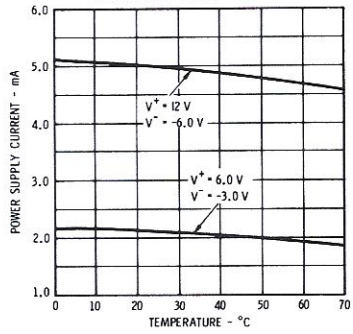
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



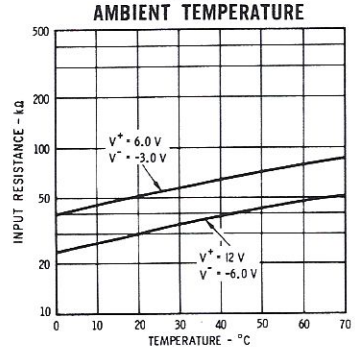
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



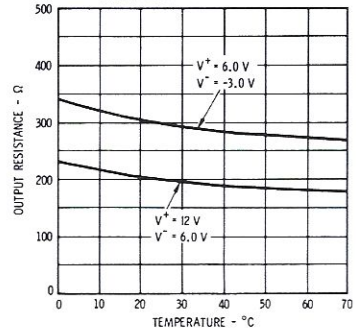
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



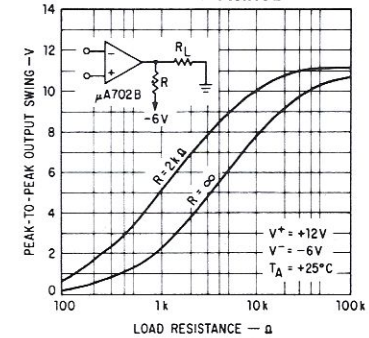
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

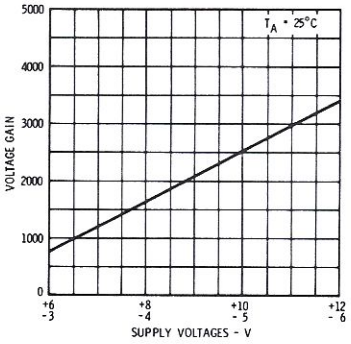


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

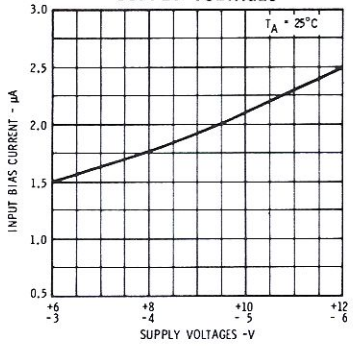


TYPICAL PERFORMANCE CURVES

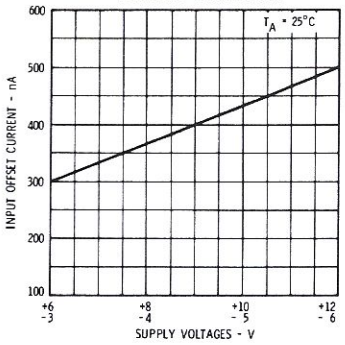
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



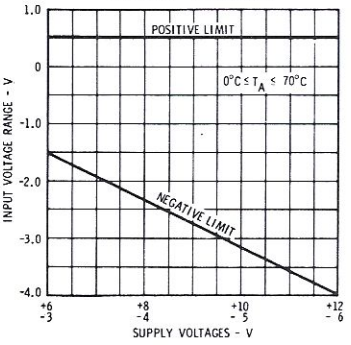
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



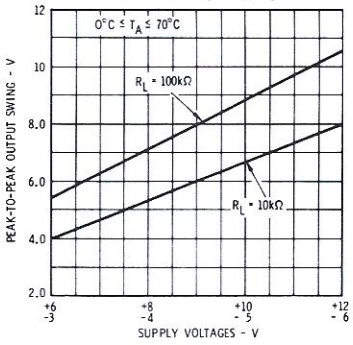
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



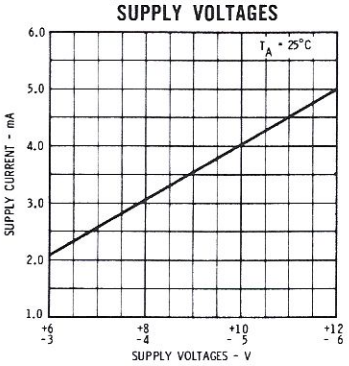
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



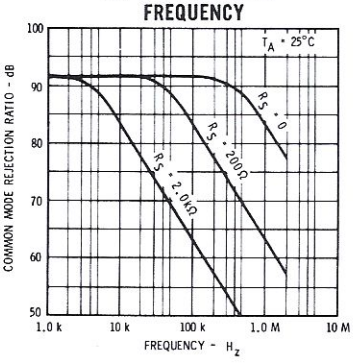
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



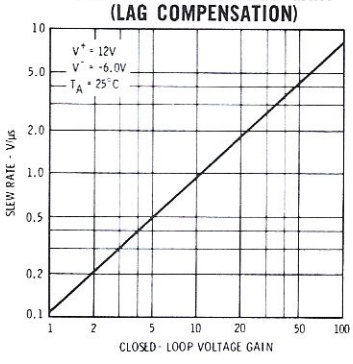
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



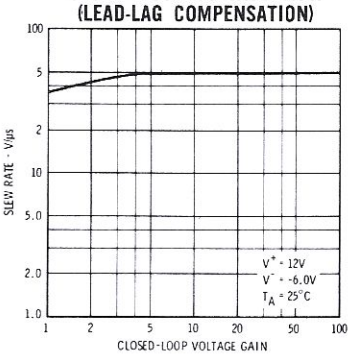
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

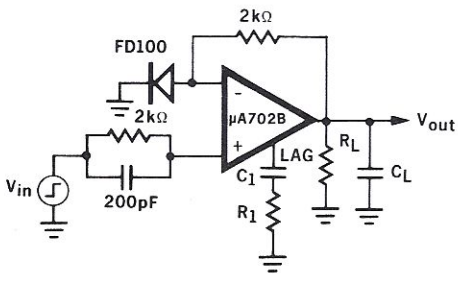


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

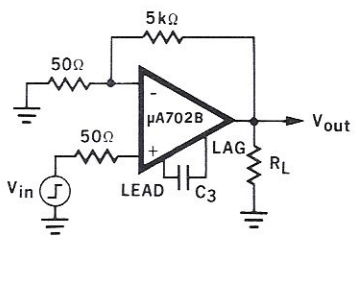


TRANSIENT RESPONSE TEST CIRCUITS

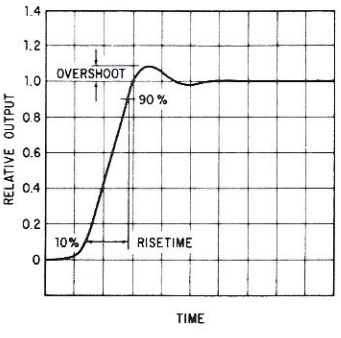
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

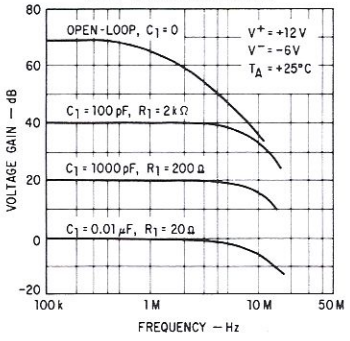
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

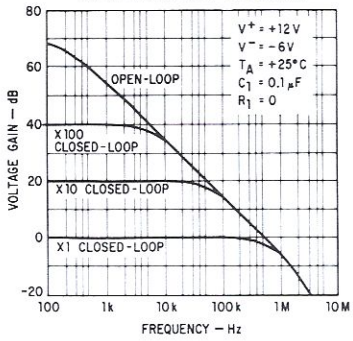
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

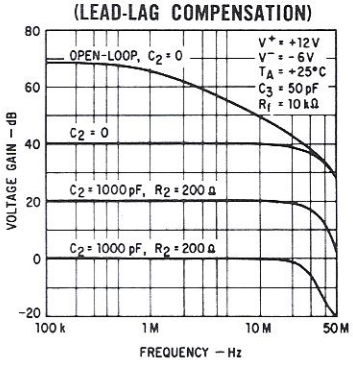
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



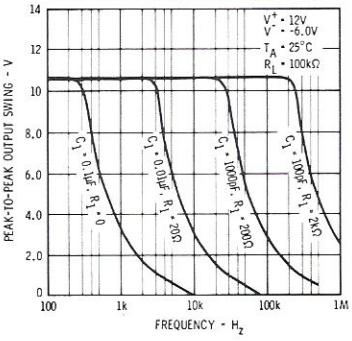
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

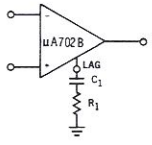


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

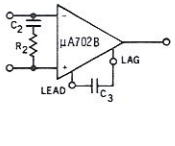


FREQUENCY COMPENSATION CIRCUITS

(Refer to Fairchild APP-117 for further details)

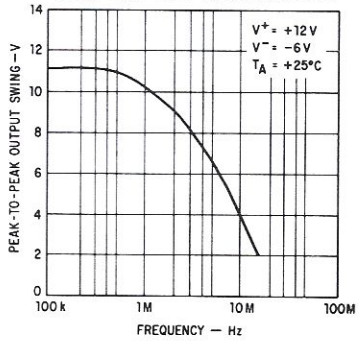


LAG COMPENSATION



LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



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